Carrier mobility in field effect transistors based on copper- phthalocyanine thin films with different phase structure

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Using annealing procedure at different temperatures after deposition at room temperature we obtained copper- phthalocyanine (CuPc) thin films with α – and β –phase structure. A phase structure of thin films was controlled by X-ray diffraction method, morphology was controlled by SEM. The field effect transistors was fabricated by high vacuum deposition of CuPc thin film (thickhess of 100 nm) on SiO_2 substrate which acting as gate contact. Gold drain and source contacts deposited on the top of active layer of FET. From measured current voltage measurements calculated mobility and concentration of charge carriers in FET. These parameters depend on phase structure of CuPc thin film, and characteristics of our FET are comparable with values of other authors.

CuPc is commercially available macro cyclic metal complex that can be easily obtained in large quantity and high purity. Together with other phthalocyanine derivatives, the chemically and thermally stable CuPc has wide applications in dye processing, spectral sensitization, chemical sensors, and optical data storage [3-4]. The semiconducting behavior of metal phthalocyanines was first observed in 1948 and they have since attracted great interest in advancement of protptype organic semiconductors. Among the metal substituted phthalocyanines CuPc has been found superior properties [5-7], such as phenomena of field dependent and wavelength-dependent efficiency in an organic static induction transistors, and stabilizing role of CuPc layer on a highly stable organic electroluminescent device based on thin film Alq, and indicated a very weak interaction between CuPc and Au at the interface.

In general, phthalocyanine materials can exist in several crystalline polymorphs, including α-, β - , x-and γ – structure, and the most well known are the thermally metastable α- and β - [8-10]. Phthalocyanine films deposited at room temperature usually consist of α-phase crystallites (at sublimation pressure of less than 10^3 Pa). At higher deposition pressures or at substrate temperature above 210°C, the β –phase directly obtained [11]. Although it is well known that α-phase crystallites undergo a phase transformation into β –phase by treatment in various organic suspension media [12,13] or during annealing at higher temperatures [14,15], only some authors describe the nature of the α→β phase transformation of copper phthalocyanine thin films with a thickness of less than 100 nm [8, 14-15].

1. INTRODUCTION

The field-effect transistors based on CuPc

Organic field effect transistors (OFETs) have attracted much attention because of their potential applications in organic/molecular electronics. Many research papers dedicated to improving characteristics of OFETs composed on CuPc thin film [16-21]. Intrinsic properties of CuPc thin film such as crystal structure, microstructure of grains, band gap and thickness influence on characteristics of OFET device. In Ref [16] investigated the charge carrier mobility of FET based on CuPc thin films on dependence of substrate temperature sustained during deposition of thin films. A highest mobility of 0.02 cm^2/V was attained when the substrate temperature of deposition was 125°C. The results of Ref [17] show the effect of CuPc morphology at different substrate temperatures on the organic FET performance. When the substrate temperature of deposition of CuPc is 120°C, a mobility of $3.75 \cdot 10^{-3}$ $cm^2/(V \cdot s)$ can obtained, which is highest value of mobility in that experiment. The electron accumulation-mode was appeared in FET based on CuPc thin film with using Ca source-drain electrodes [19]. At the same time that device also showed a p-channel and typical ambipolar transistor properties. The filed-effect electron mobility of 1.010^{-3} $cm^2/(V \cdot s)$ and filed-effect hole mobility of $2.5 \cdot 10^{-3}$ $cm^2/(V \cdot s)$ were estimated from the saturation currents above the threshold voltage [19]. The device properties of CuPc based bottom contact thin-film transistor depends on active layer thicknesses, and device with a CuPc layer of 80 nm showed the maximum filed effect mobility [20].

The carrier mobility of thin film transistor based on CuPc depends on the morphology of layer thickness [21] Among FETs based on CuPc a highest mobility of 0.1-0.2 $cm^2/(V \cdot s)$ was achieved in the transistor which based on individual single-crystalline sub micrometer sized ribbons [22]. Some scientific group fabricated organic FETs with polymer gate dielectric films

such as poly-*p*- xylylene and polymethyl methacrylate [18,23].

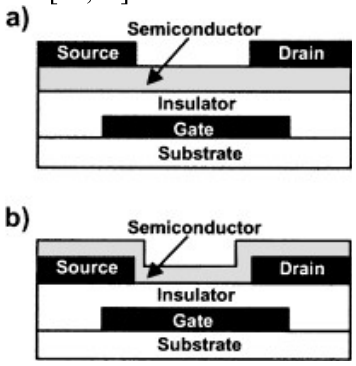


Figure1. OTFT device configurations:
a) Top-contact device, with source and drain electrodes evaporated onto the organic semiconducting layer through a mask.
b) Bottom-contact device, with the organic semiconductor deposited onto the gate insulator and the prefabricated source and drain electrodes.

Figure1 shows two common device configurations used in OFTs. The *I-V* characteristics of organic FETs can be adequately described by models developed for inorganic semiconductors [24] and shown earlier [25-30].

Let us consider thin film transistor with channel length and width of L and W, respectively, and gate insulator thicknesses d_{ox} . The active layer material is assumed to be unintentionally p –doped and in the on state one has a p-accumulation channel with the hole mobility μ. In the most simple model [31], named as the Shockley model the (above threshold) source - drain current (I_{DS}) of the transistor depends on source – drain and gate–source voltages V_{DS} and V_{GS}, respectively, as

$$I_{DS} = \begin{cases} \mu \frac{W}{L} C_{ox} \left[(V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] & when\ V_{DS} < V_{GS} - V_{th}; \\ \mu \frac{W}{L} \frac{1}{2} C_{ox} (V_{GS} - V_{th})^2 & when\ V_{DS} > V_{GS} - V_{th}. \end{cases} \quad (1)$$

Here V_{th} is the threshold voltage and $C_{ox} = \varepsilon_0 \varepsilon_{ox}/d_{ox}$ is the insulator capacitance per unit area. Then ε_0 is the dielectric permittivity of vacuum and ε_{ox} is the dielectric permittivity of insulator. Evidently, all material properties in these equations are the mobility and threshold voltage, whereby the latter can be influenced also by the interface to the gate insulator. When V_{GS} is smaller than the sum of V_{th} and V_{DS} , the depletion layer is enhanced around drain electrode and I_{DS} does not increase (pinch-off). Source- drain current I_{DS} after the occurrence of pinch-off effect named as saturation current and expressed by second formula of equation system (1). According that mobility of carriers μ can be obtained by plotting $\sqrt{I_{DS}^{sat}}$ against V_{GS}, i.e.

$$\sqrt{I_{DS}^{sat}} = \sqrt{\frac{1}{2} \frac{W}{L} \mu C_{ox}}\ (V_G - V_{th}). \quad (2)$$

We can calculate electrical parameter such as electric conductivity σ and carrier concentration N_p by

$$\sigma = \frac{L}{W d_{ox}} \cdot \frac{dI_{DS}}{dV_{DS}}\Big|_{V_{GS}=0}; \quad (3)$$

$$N_p = \frac{\sigma}{q\mu}. \quad (4)$$

Where q is elementary electric charge.

2. EXPERIMENTAL PROCEDURE

2.1. Sample preparation

CuPc powder was purchased from Aldrich Chemical Co. and used without further purification. The CuPc thin films are fabricated by the standard vacuum evaporation technique. In this investigation CuPc thin films were evaporated on different substrates such as slide glass and Si_2O layer coated on high doped silicon. The glass substrate was cleaned by acetone, ethyl alcohol and distilled water.

The CuPc thin films are fabricated by the standard vacuum evaporation technique. A Cu-Pc source, contained in a ceramic crucible, was resistively heated in high vacuum chamber at 10^{-7} Torr. The deposition rate was controlled at 0.02 - 0.05 nm/sec. The resulting films were about 100 nm thick with deposition rate and thickness monitored by a thickness monitor. The deposition rate and thickness were monitored by a thickness monitor. During deposition substrate temperature was 25 °C (room temperature).

In order to study the effect of annealing on the

characteristics of CuPc films deposited on glass substrate, three samples were prepared: as deposited thin film, films after annealed at 200 °C and 350 °C for 1 hour, respectively.

For conductivity measurements gold contacts were deposited on the surface of the CuPc thin films with a thickness of 300 nm and a channel length of 50 μm.

Top contact field effect transistors with CuPc thin film active layer were fabricated on Si_2O layer, which was coated on high doped silicon. Gold was vacuum deposited through a shadow mask to form electrodes on the CuPc surface, and transistor channel length and width were 50 nm and 3 mm. The thickness of Si_2O insulator layer was 1 mm. Gold gate contact was evaporated on n^+ doped Si_2O insulator layer.

2.2. Experimental setup

The optical absorption of the CuPc thin films was measured in the range 450-850 nm using a SCINCO UV-Vis spectrometer. The change of the crystal structure of CuPc thin films was inspected by x-ray diffraction. Surface morphology of the films was characterized by a scanning electron microscope (SEM). The temperature dependence of conductivity of thin films was measured by a source meter (Keithley 2400).

3. RESULTS AND DISCUSSION

3.1. A phase structure of CuPc thin film.

Figure 3 shows the optical absorption spectra of CuPc thin films deposited on the glass substrate at room temperature and after annealed at different temperatures for 1 hour. As shown in Figure 2, for the absorption spectra of the as-deposited thin film (RT) the higher energy maximum peak is larger than that of the second peak. Similar behavior is shown by the thin film annealed at 200 °C. This behavior represents the typical features of the α-phase of CuPc thin films. As the annealing temperature increased to 350 °C, the peak positions were changed to the maximum peaks positions of the β-phase of CuPc [18,19].

Figure 3 shows the x-ray diffraction patterns for Cu-Pc thin films annealed at different temperatures. CuPc thin films deposited at room temperature showed only two distinct peaks at 6.7° and 13.5°, corresponding to the (002) and (400) lattice plane of the α-phase of CuPc. At the annealing temperature of 200 °C, five peaks corresponding to the crystal structure of the α-phase of CuPc were observed. CuPc thin films annealed at 350 °C showed the distinct eight peaks corresponding to the β-phase[20].

From optical absorption spectra and X-ray data we conclude that CuPc thin films deposited at room temperature has semi disordered α-phase structure, but thin films after annealed at 200 °C and 350 °C have α- and β-phase structure.

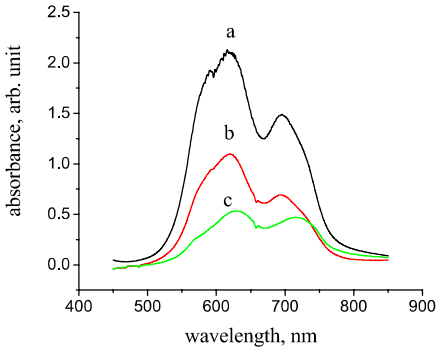


Figure 2. Optical absorption spectra of CuPc thin films : a- deposited at RT ; b- annealed at 200 ℃; c- annealed at 350 ℃.

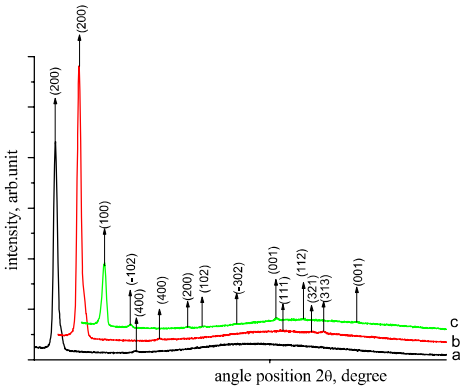
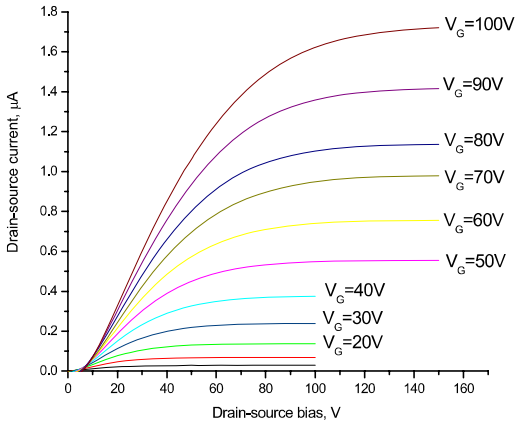


Figure 3. X-ray diffraction spectra of CuPc thin films : a- deposited at RT ; b- annealed at 200 ℃; c- annealed at 350 ℃.

3.2. FET on CuPc thin film.

We measured output characteristics of top contact FET (see Figure 1:a) based on CuPc thin films, which treated by different procedures such as deposition at RT, in-situ annealing at 200 °C and 350 °C for 1 hour after deposition at RT. Figure 4 shows output characteristics of investigated FETs. Also shown graph (Figure 4:d) of square root of saturated drain-source current on dependence of gate bias for FETs. With using that dependencies by equations (2)-(4)

were calculated electrical parameters of CuPc layers, which given in Table 1.



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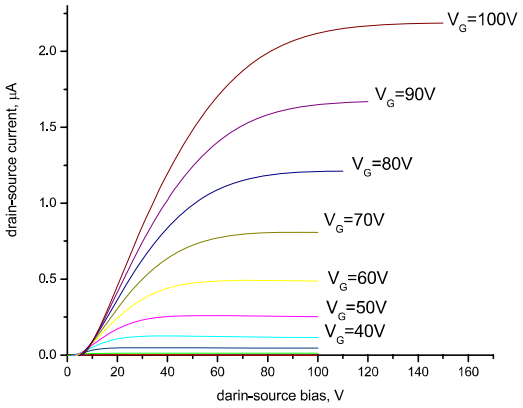

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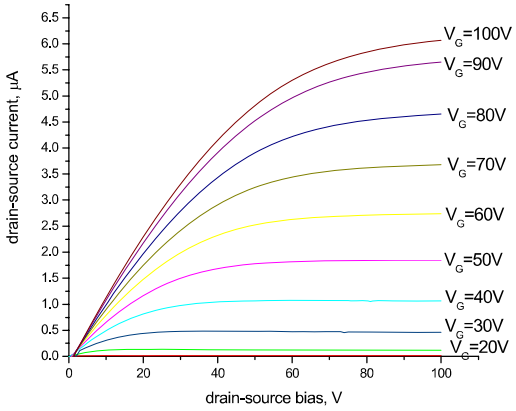

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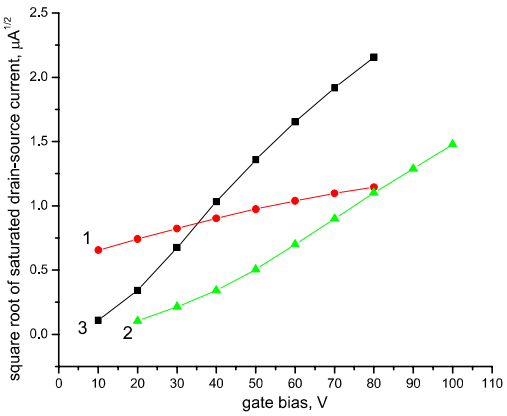

d

Figure 4. Output characteristics of FETs based on CuPc thin films treated by different procedures: a- deposited at RT;b- annealed at 200°C; c-annealed at 350°C; d- graph of $(I_{DS})^{1/2}$ vs. gate voltage for FETs (1- deposited at RT, 2 - annealed at 200°C; 3 - annealed at 350°C).

Table 1. Electrical parameters of CuPc thin films obtained from FET characteristics.

Thin film treatment	Mobility, $cm^2/(V\cdot s)$	Conductivity, S/cm	Concentration of carriers, cm^{-3}	Threshold voltage, V
Deposited at RT	$6.6\cdot10^{-4}$	$2.33\cdot10^{-6}$	$2.2\cdot10^{16}$	13.4
Annealed at 200°C	$1.54\cdot10^{-3}$	$4.17\cdot10^{-7}$	$1.7\cdot10^{15}$	-18.41
Annealed at 350°C	$4.51\cdot10^{-3}$	$6.57\cdot10^{-8}$	$9.1\cdot10^{13}$	-6.9

The field effect mobility of FET based on CuPc thin films changes by annealing procedure. FET based on as-deposited CuPc thin film has the lowest value, which close to results of Ref. [16-21]. But our value higher than results of Ref. [31,32], where the mobility FET based on as grown undoped CuPc thin film has an order of magnitude of 10^{-10}~10^{-9} $cm^2/(V \cdot s)$. In result of annealing at 200°C for 1 hour applied on CuPc thin film the field effect mobility of transistor increased about 2.3 times. The field effect mobility of CuPc deposited at room temperature also increased after annealing 100°C for 1 hour [31]. In our investigation the transistor based on CuPc thin film annealed at 350° for 1 hour after deposition has most high value of field effect mobility, which is 6.9 time higher than that of transistor based on as deposited CuPc thin film. This value is comparable with highest values achieved in Ref. [17,19-21], but lower on one order than result of Ref. [16]. As it is above mentioned, among FETs based on CuPc a highest mobility of 0.1-0.2 $cm^2/(V \cdot s)$ was achieved in the transistor which based on individual single-crystalline sub micrometer sized ribbons [22]. Threshold voltages of our FETs based on CuPc thin films comparable with data of other authors [16,18,19, 21].

In result of annealing procedures acted after deposition at temperatures 200°C and 350°C for 1 hour the conductivity and concentration of charges on CuPc thin films significantly decreased (Table 5). It is known, that the annealing procedure at 350°C for 2 hours after deposition decreased ratio of free carrier concentration to free carrier effective mass in SnPc thin films 1.63 times [60]. The decrease of carrier concentration we can explain, that in result of annealing procedure grains of CuPc thin film merge and grow, and consequently number of the acceptor impurities on grain boundaries decrease.

4. CONCLUSION

We fabricated FET based on CuPc thin films, which annealed at different temperature after deposition at RT. Characteristics of our FET are comparable with values of other authors. Shown that annealing procedure applied on CuPc thin film influences on electrical parameters of FET. In result of annealing at 200°C for 1 hour applied on CuPc thin film the field effect mobility of transistor increased about 2.3 times. In our investigation the transistor based on CuPc thin film annealed at 350° for 1 hour after deposition has most high value of field effect mobility, which is 6.9 time higher than that of transistor based on as deposited CuPc thin film. Thus, FET based on CuPc thin film with β – phase crystal structure has mobility of carriers of $4.51 \cdot 10^{-3}$ $cm^2/(V \cdot s)$, which is comparable with highest values achieved by other researchers. In result of annealing procedures acted after deposition at temperatures 200°C and 350°C for 1 hour the conductivity and concentration of charges on CuPc thin films significantly decreased.

5. ACKNOWLEDGEMENTS

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